## REMARKS

Claims 1-3, and 5-25 are pending in this application. Claim 4 has been canceled, and claims 22-25 have been newly added. Reconsideration of the rejections in view of the amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

**Rejections under 35 USC §112, Second Paragraph**

Claims 8-13 were rejected under 35 USC §112, second paragraph, as being indefinite because the terms "relatively thick" and "relatively thin" in claim 8 are relative terms.

Claim 8 has been amended to overcome the rejections.

**Rejections under 35 USC §102(b)**

**Claims 1 and 2 stand rejected under 35 USC §102(b) as being anticipated by Sekiguchi et al (U.S. Patent No. 5,780,908).**

Applicant respectfully traverses this rejection.

Sekiguchi et al, e.g., in Figs. 3a to 3d, forms a second insulating film 4, making a contact hole 5 through the second insulating film 4, forming a plug of tungsten in the contact hole, and then nitriding the surface of tungsten plug 7 to form tungsten nitride layer 7b. Then, an aluminum alloy film 8a is formed on

the second insulating film, and is connected to the tungsten plug 7. Thus, Sekiguchi et al discloses a formation of an aluminum wiring on the tungsten plug.

In contrast, the present invention is directed to a method adapted to form a memory device having a capacitor. The manufacturing step of a capacitor includes a process in an oxidizing atmosphere. For protecting a tungsten plug from oxidization, the upper part of the tungsten plug is nitrided to form the tungsten nitride.

Claim 1 has been amended to further recite the steps of "(e) forming an etch stopper layer on the first insulating film, the etch stopper layer covering the plug" and "(f) forming a second insulating film on said etch stopper layer," also to recite "wherein said etch stopper layer has a function of etch stopper in etching said second insulating film." These steps make it possible to form a capacitor having a rare metal electrode and an oxide dielectric layer, which is not taught or suggested in Sekiguchi et al.

Therefore, Sekiguchi et al does not teach or suggest, among other things, "(e) forming an etch stopper layer on the first insulating film, the etch stopper layer covering the plug; and (f) forming a second insulating film on said etch stopper layer, wherein said etch stopper layer has a function of etch stopper in etching said second insulating film," as recited in claim 1.

For at least these reasons, claim 1 patentably distinguishes over Sekiguchi et al. Claim 2, depending from claim 1, also patentably distinguishes over Sekiguchi et al for at least the same reasons.

Thus, the 35 USC §102(b) rejection should be withdrawn.

**Claims 1-5, 8 and 10-12 stand rejected under 35 USC §102(b) as being anticipated by Saenger et al (U.S. Patent No. 5,633,781).**

Applicant respectfully traverses this rejection.

The Examiner has alleged that Saenger et al teaches heating the semiconductor substrate in a nitriding atmosphere to nitride the plug. Such a disclosure cannot be found. The referred portion in Saenger et al merely describes that "conductive plug 6 has been formed by a conventional process... and may be... W...," and "electrically conductive diffusion barrier 8 was formed... and may be $Ta_{1-x}Si_xN_y$, TiN, or similar materials."

In Saenger et al, when the plug 6 is formed of W, the diffusion barrier does not contain W, and hence cannot be formed by nitriding the plug. Nothing in Saenger et al indicates that the plug is nitrided. Even though layer 10 sandwiched between dielectric layers 12 and 14 can be formed of WN (column 4, line 22), this layer cannot be called a plug by any means.

The Examiner has also alleged that Saenger et al teaches forming an etch stopper layer on the first insulating film, the etch stopper covering the plug at column 6, lines 27-50. The referred to portion of Saenger et al describes forming a refractory metal layer on the gate, and the source/drain, which may be subjected to nitrogen containing plasma to form a refractory metal nitride on the surface of the refractory metal layer, to prevent inter-diffusion of the refractory metal layer and the interconnect to be formed later. These descriptions are not regarding the plug.

The Examiner alleged that Saenger et al discloses forming a second insulating film on the silicon nitride layer, forming an opening through the second insulating film, the opening reaching the surface of the

plug, forming rare metal layer in the opening (Figs. 10-15, column 6, lines 20-65). Even assuming that the layer 52 is an etch stopper layer, and that the dielectric layer 14 formed thereon correspond to the second insulating film, the plug 6 is formed of tungsten, etc, but is not covered with a tungsten nitride film. Tungsten itself is exposed in the contact hole. Therefore, if oxidizing atmosphere touches plug 6, the surface of plug 6 will be oxidized.

In the present invention, the surface of a plug embed in the insulating film is nitrided to form metal nitride, the surface of which is covered with an etch stopper layer. Saenger et al does not teach or suggest such a feature.

Thus, Saenger et al does not teach or suggest, among other things, "(d) **heating the semiconductor substrate in a nitriding atmosphere to nitride the plug from a surface thereof**; (e) **forming an etch stopper layer on the first insulating film, the etch stopper layer covering the plug.**"

For at least these reasons, claim 1 patentably distinguishes over Saenger et al. Claims 2, 3 and 5, depending from claim 1, also patentably distinguishes over Saenger et al.

With regard to claim 8 of the present invention, the Examiner appears to allege that Saenger et al discloses forming a dielectric film on a surface of the lower electrode by CVD. The Examiner does not refer to the teaching that the dielectric layer is made thick at the region near a boundary between the top surface and each of the side surfaces.

In the structure of Saenger et al shown in Figs. 2A to 2H, side wall conductive spacers 28, 16 are formed on the side-walls of an aperture in the stacked structure, and the dielectric spacers 18 of high

dielectric constant are formed thereon. The dielectric layer 18 does not have an increased thickness at the top part. The dielectric layer 18 does not cover the side surfaces, but covers only one side surface.

Thus, Saenger et al does not teach or suggest, among other things, "(b) forming a dielectric film on a surface of the lower electrode, **the dielectric film in a region near a boundary between the top surface and each of the side surfaces being thicker than the dielectric film in a lower region of the side surfaces.**"

For at least these reasons, claim 8 patentably distinguishes over Saenger et al. Claims 10-12, depending from claim 8, also patentably distinguishes over Saenger et al.

Thus, the 35 USC §102(b) rejection should be withdrawn.

**Claims 15-20 stand rejected under 35 USC §102(b) as being anticipated by Joo (U.S. Patent No. 6,345,425).**

Applicant respectfully traverses this rejection.

Joo teaches forming a rare metal layer above a semiconductor substrate, forming an insulating mask layer on the rare metal layer, and patterning rare metal using a patterned insulating mask layer. The insulating mask layer is not shown in the figures, and is only referred to in the description that the rare metal can be patterned using a hard mask. It is presumed that such a hard mask is also removed after the patterning process. It should be noted that, in the present invention, the insulating mask layer is not removed, but it is instead used as part of the insulating layer.

Therefore, Joo does not teach or suggest, among other things, "(f) **forming an insulating film over the semiconductor substrate, the insulating film covering the patterned insulating mask layer**." as recited in claim 15.

For at least these reasons, claim 15 patentably distinguish over Joo. Claims 16-20, depending from claim 15, also patentably distinguish over Joo for at least the same reasons.

Thus, the 35 USC §102(b) rejection should be withdrawn.

**Rejections under 35 USC §103(a)**

**Claim 3 stands rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al in view of Foster et al (U.S. Patent No. 5,567,243).**

Applicant respectfully traverses this rejection.

As discussed above, claim 1 patentably distinguish over Saenger et al. Foster et al, cited for allegedly disclosing the nitriding process using ammonium and a temperature between 600°C and 850°C, does not remedy the above deficiencies of Saenger et al.

For at least these reasons, claim 15 patentably distinguish over the cited references.

Thus, the 35 USC §103(a) rejections should be withdrawn.

**Claims 6, 9 and 13 were rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al in view of Applicant admitted prior art.**

Applicant respectfully traverses this rejection.

As already discussed above, claims 1 and 8 patentably distinguish over Saenger et al. Applicant admitted prior art, cited for allegedly disclosing forming the rare metal layer by sputtering followed by a CVD process using oxygen. and the lower electrode having a cylinder shape as conventional in the art, does not remedy the above deficiencies of Saenger et al.

For at least these reasons, claim 6, depending from claim 1, and claims 9 and 13, depending from claim 8, patentably distinguish over the cited references.

Thus, the 35 USC §103(a) rejections should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is respectfully requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/765,437**



**IN THE TITLE:**

SEMICONDUCTOR DEVICE HAVING A CAPACITOR WITH RARE METAL ELECTRODE

**IN THE CLAIMS:**

Claim 4 has been canceled.

Claims have been amended as follows:

1. (Amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a first insulating film above a semiconductor substrate formed with semiconductor elements;

(b) forming a contact hole through the first insulating film;

(c) forming a plug made of conductive material capable of being nitrided, the plug being embedded in the contact hole; ~~and~~

(d) heating the semiconductor substrate in a nitriding atmosphere to nitride the plug from a surface thereof ;

(e) forming an etch stopper layer on the first insulating film, the etch stopper layer covering the plug; and

(f) forming a second insulating film on said etch stopper layer,

12 wherein said etch stopper layer has a function of stopping etching of said second insulating film.

5. (Amended) A method of manufacturing a semiconductor device according to claim ~~4~~ 1, wherein said step (e) includes a step of heating the semiconductor substrate and supplying SiN source gas to the semiconductor substrate to form an SiN layer on the first insulating film through chemical vapor deposition, the SiN layer covering the plug.

8. (Amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a lower electrode above a semiconductor substrate formed with semiconductor elements, the lower electrode having a top surface and side surfaces;

(b) forming a dielectric film on a surface of the lower electrode, the dielectric film ~~being relatively thick~~ in a region near a boundary between the top surface and each of the side surfaces ~~and relatively thin and generally uniform~~ being thicker than the dielectric film in a lower region of the side surfaces; and

(c) forming an upper electrode on the dielectric film.

15. (Amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a rare metal layer above a semiconductor substrate formed with semiconductor elements;

(b) forming an insulating mask layer on the rare metal layer;

(c) patterning the insulating mask layer by using a resist pattern; ~~and~~

(d) pattering the rare metal layer by using the patterned insulating mask layer; and

(f) forming an insulating film over the semiconductor substrate, the insulating film covering the patterned insulating mask layer.

19. (Amended) A method of manufacturing a semiconductor device according to claim 15, further comprising the steps of:

(g) annealing the semiconductor substrate in hydrogen-containing gas.